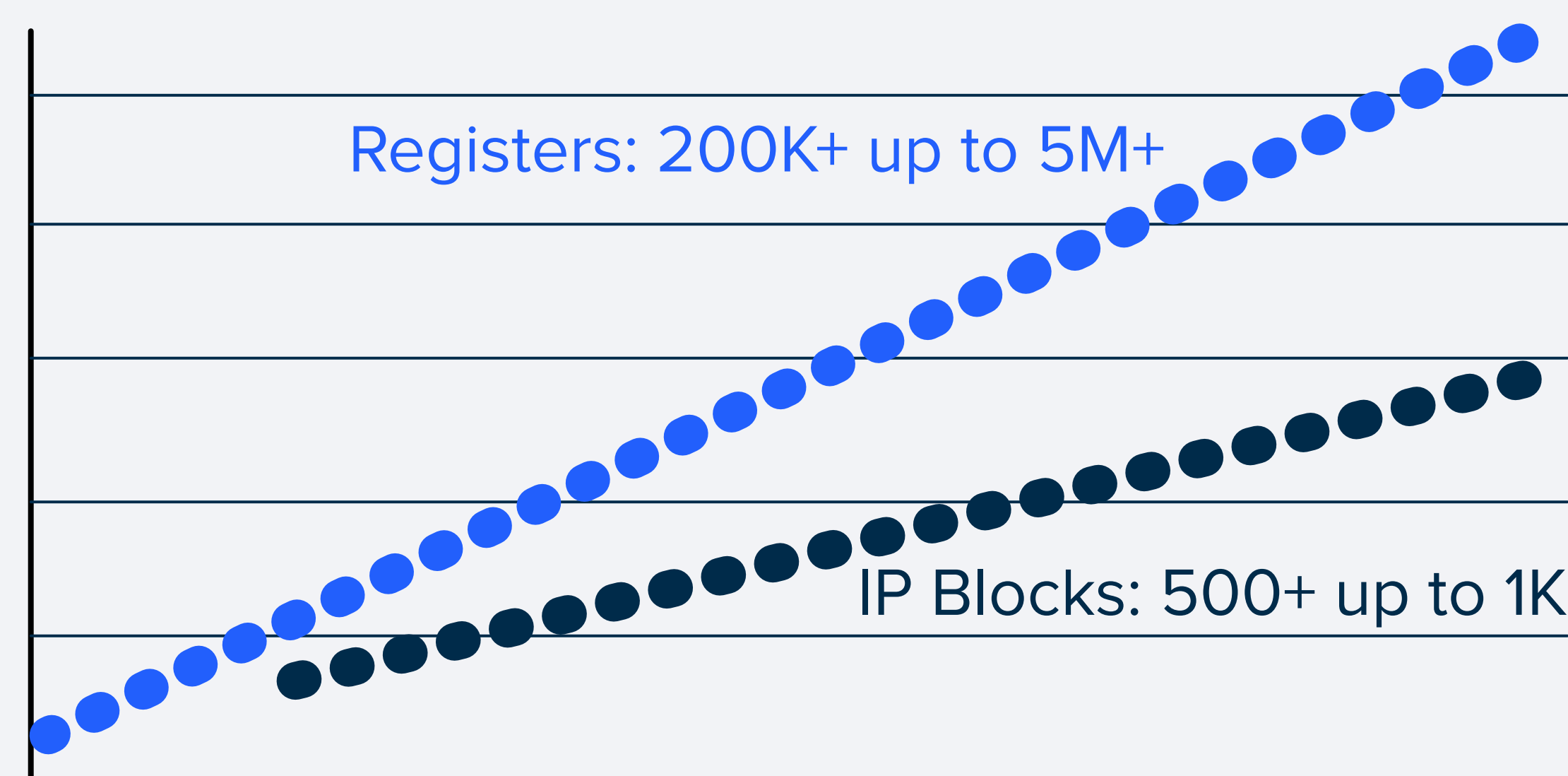


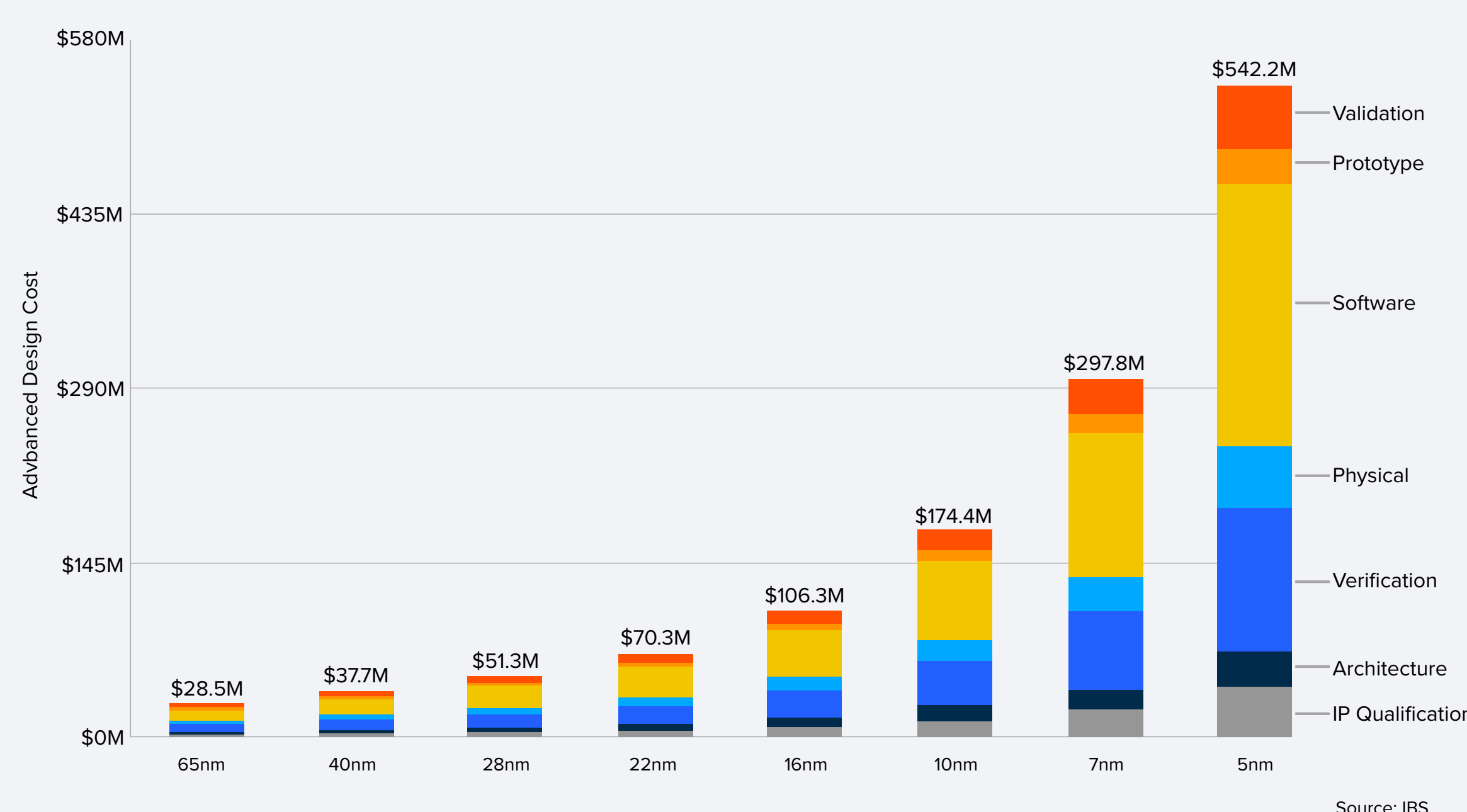
A Single Source Unified Approach to CSR Register Development

Challenge

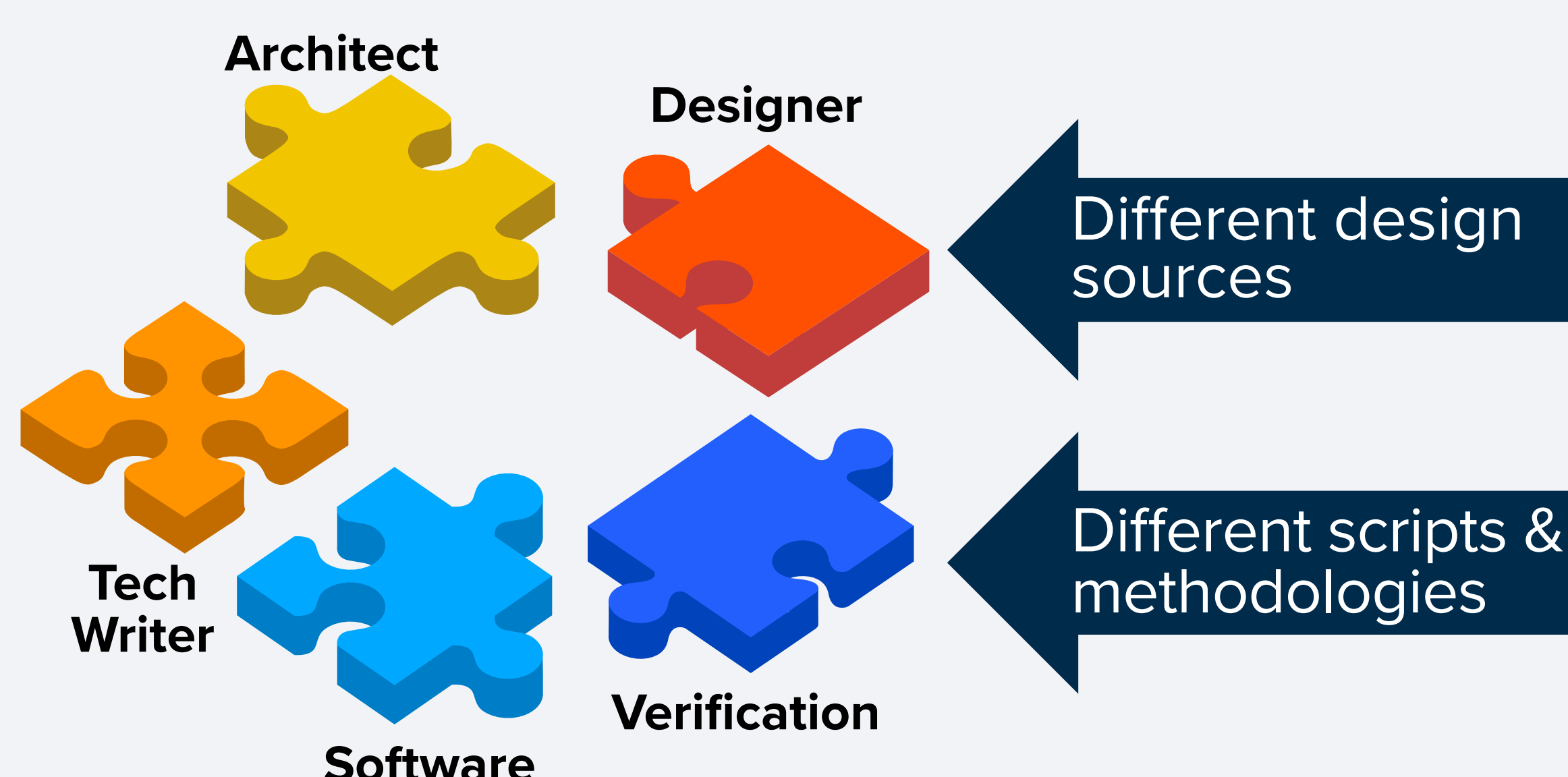
Design complexity has outgrown manual workflows
Hardware Software Interfaces (HSIs) are critical to design success



Developing complex SoCs is expensive, efficiencies are critical to cost control



Team silos and serial design process leads to specification misalignment, respins and costly designs



Resolution

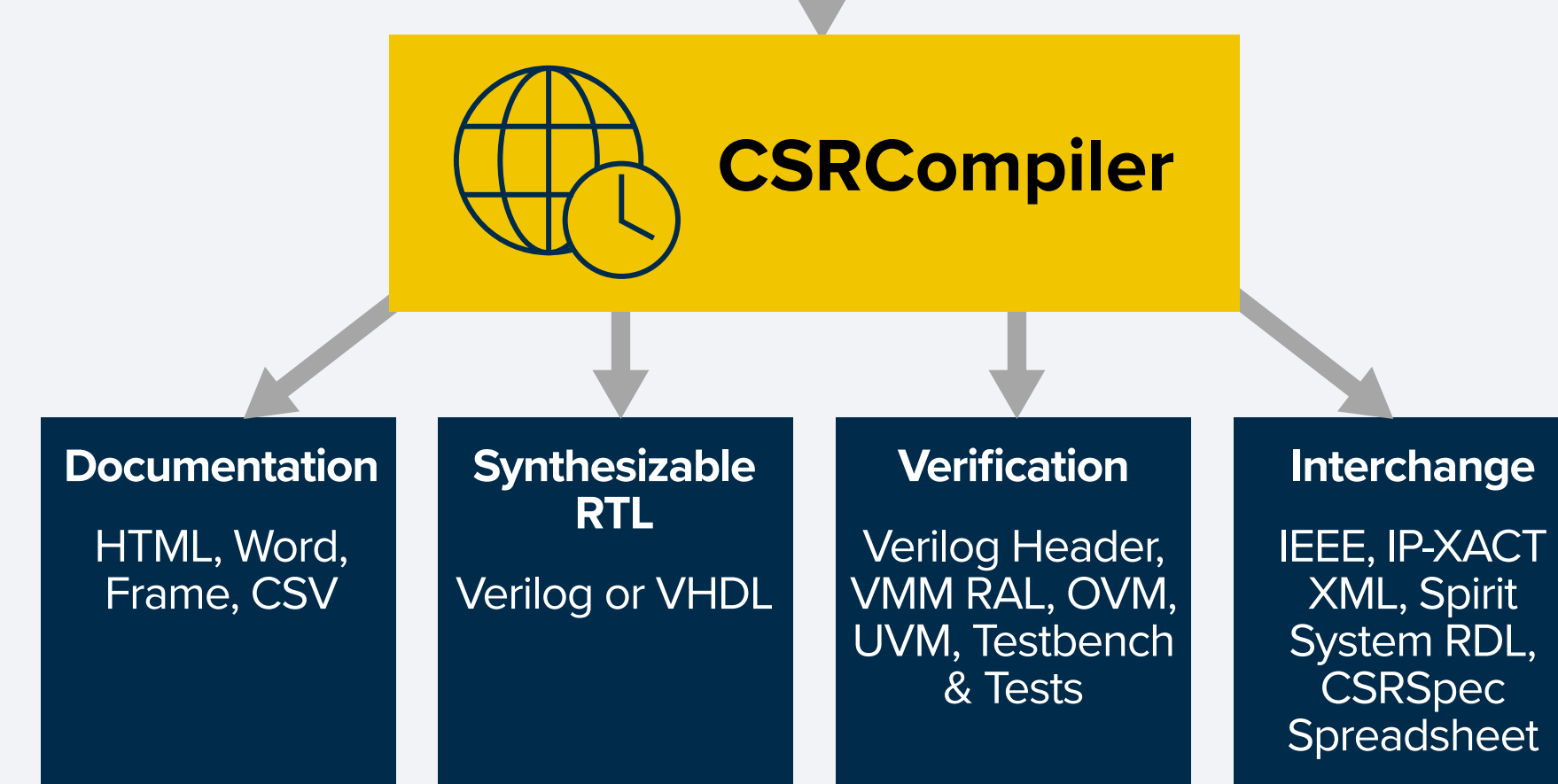
Automate Hardware Software Interface (HSI) with CSRCompiler from Arteris – a new technology for a winning methodology

Unified Specification and Compilation Flow

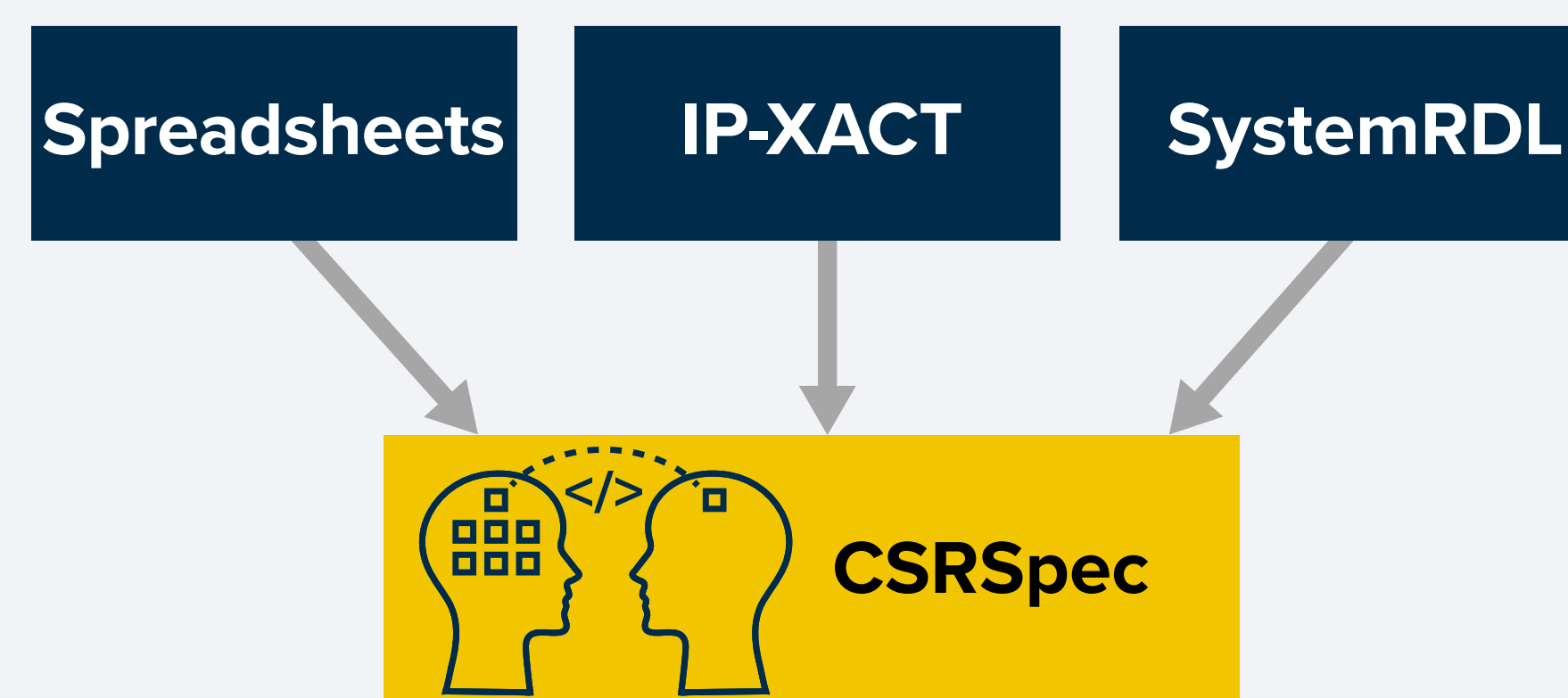
- Automate the generation of all outputs
- Eliminate time-consuming and error-prone manual scripting and editing of design data
- Rapid, highly iterative design environment for largest, most complex designs through a scalable infrastructure

Iterations to update the specification and generate the new outputs

Single Source Register Specification:
CSRSpec, SystemRDL, Spreadsheet, or IEEE IP-XACT



Domain-Specific Language to Specify All Aspects of the HSI



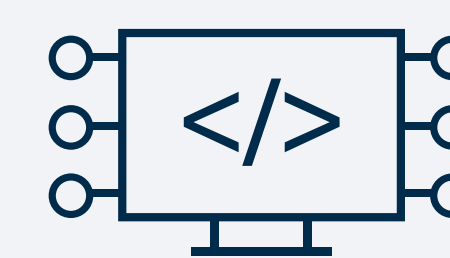
- A single data source to generate RTL, firmware headers, verification class instances, and documentation outputs
- Over 200 unique properties and 6,000 register behavior combinations and address map hierarchy description
- Repeatable, scalable, legacy data reuse
- Support for industry standards and those not currently available (bus, memory, wide data paths)
- Advanced capabilities include atomic access for wide registers and register aliasing and broadcasting

CSRCompiler Benefits



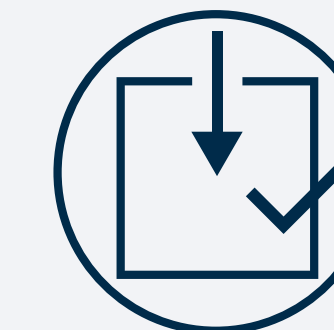
Agile Design Process

Ensure best practices and early engagement of the entire design process



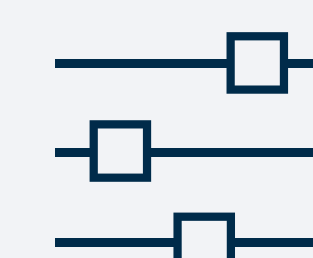
Multi-Language Support

No need for additional custom scripting or manual post-processing



Identify IP Issues

Ensure clean import of third-party IP or internal legacy data



Easy Specification Adjustment

Very fast iteration with updated information across design teams ensuring data consistency



Highest Capacity

Specify and compile over 5 million registers



Highest Quality RTL

Over 1,000 functional behavioral, syntactic, and semantic error checks

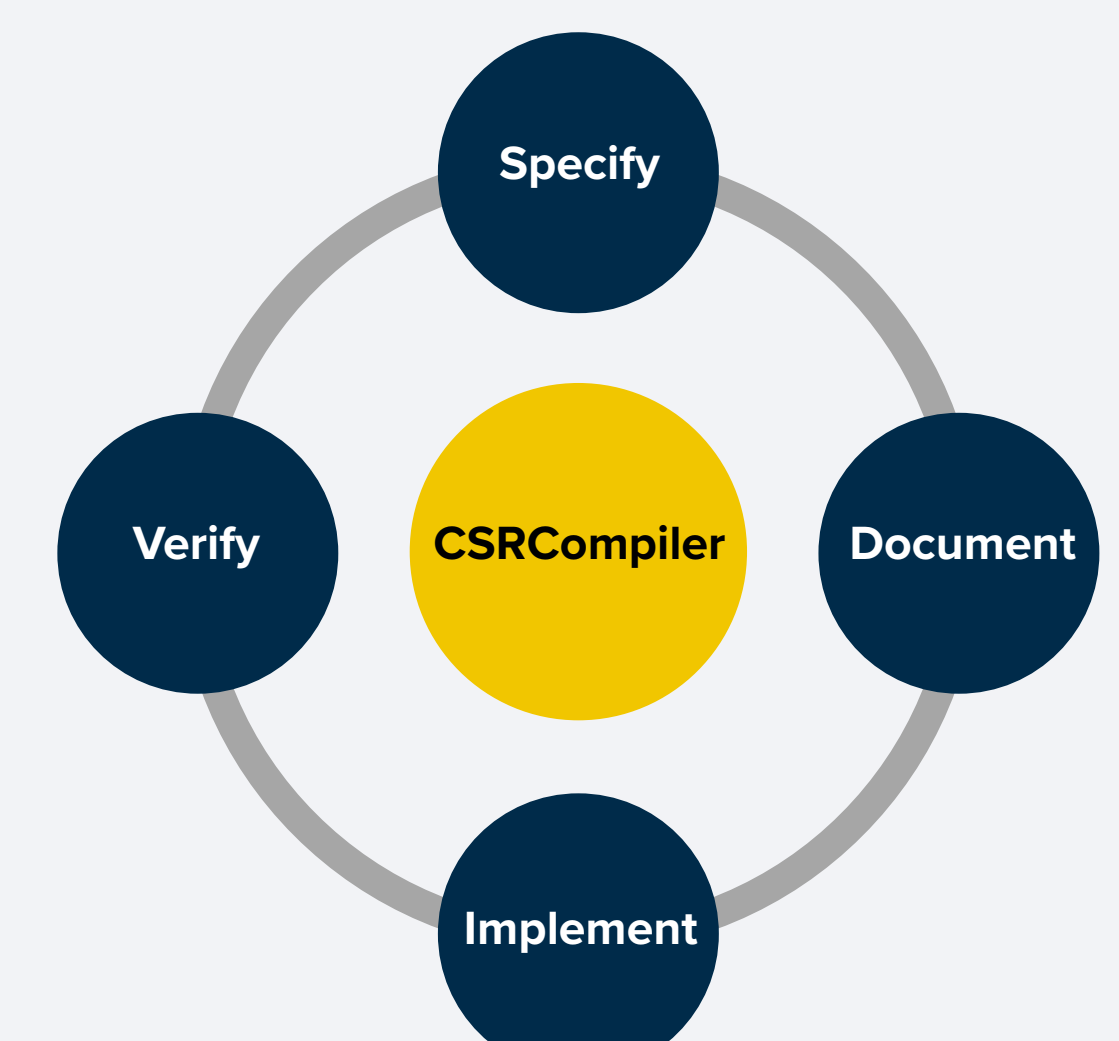


Fastest Performance

Generate 100,000 registers in seconds

Use Case

- 336K CSRs with almost 900K fields
- Representing 5% of the total die area
- 600+ discrete CSR files, various formats



Results:
Number of manually maintained CSR specifications **reduced by over 60x**